Amendments to the Claims

Please amend the Claims as shown below. This listing of Claims replaces all prior versions and listings of the Claims in this application.

Listing of Claims

1. (Currently Amended) A semiconductor device comprising:

a via within an insulation layer over a semiconductor substrate;

a barrier metal layer on a surface of the via;

a metal line ~~comprising~~ consisting essentially of copper in the via over the barrier metal layer having vertical side surfaces that contact the barrier metal layer;

a pad in a predetermined region of the metal line; and

an alloy layer on an upper surface of the metal line, ~~wherein~~ having a top surface ~~of the alloy layer~~ that is coplanar with or lower than a top surface of the insulation layer and vertical side surfaces that contact the barrier metal layer within the via, ~~and~~ wherein the alloy layer ~~comprises~~ consists essentially of copper and a low melting point metal selected from the group consisting of aluminum, lead, and silver.

2. (Canceled)

3. (Canceled)

4. (Previously Presented) The semiconductor device of claim 1, wherein a thickness of the alloy layer is less than a thickness of the metal line.

5. (Previously Presented) The semiconductor device of claim 1, further comprising a protection layer comprising silicon nitride or silicon oxynitride on the metal line except for the predetermined region.

6. (Canceled)

7. (Canceled)

8. (Previously Presented) The semiconductor device of claim 5, wherein a width of the pad is less than a width of the via.

9-20. (Canceled)

21. (Canceled)

22. (Previously Presented) The semiconductor device of claim 1, wherein a width of the pad is less than a width of the via.

23. (Previously Presented) The semiconductor device of claim 1, wherein the barrier metal comprises a metal selected from a group consisting of Ti, Ta, TiN, and TaN.

24. (Previously Presented) The semiconductor device of claim 1, wherein the barrier metal has a thickness between 200 and 800 Å.

25. (Canceled)

26. (Canceled)

27. (Previously Presented) The semiconductor device of claim 1, wherein the insulation layer comprises an oxide layer.

28. (Previously Presented) The semiconductor device of claim 23, wherein the barrier metal layer prevents the diffusion of copper from the metal line into the substrate.

29. (Previously Presented) The semiconductor device of claim 1, wherein the alloy layer is completely within the via.

30. (Previously Presented) The semiconductor device of claim 1, wherein the barrier metal layer covers all surfaces of the via.

31. (Previously Presented) The semiconductor device of claim 5, wherein the alloy layer is exposed through an opening in the protection layer.

32. (Previously Presented) The semiconductor device of claim 1, wherein the barrier metal has a thickness of ~500 Å.

33. (Canceled)

34. (Previously Presented) The semiconductor device of claim 1, wherein the barrier metal layer contacts the substrate.

35. (Previously Presented) The semiconductor device of claim 5, wherein the pad is exposed through an opening in the protection layer.

36. (Previously Presented) The semiconductor device of claim 1, wherein the alloy layer comprises copper and aluminum.

37. (Previously Presented) The semiconductor device of claim 1, wherein the alloy layer comprises copper and either lead or silver.